FIG. 1A
PRIOR ART

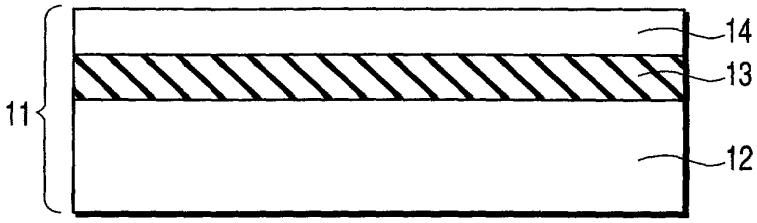


FIG. 1B
PRIOR ART

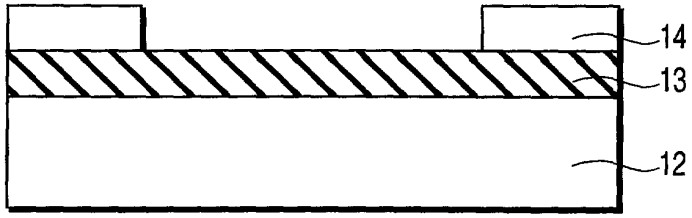


FIG. 1C
PRIOR ART

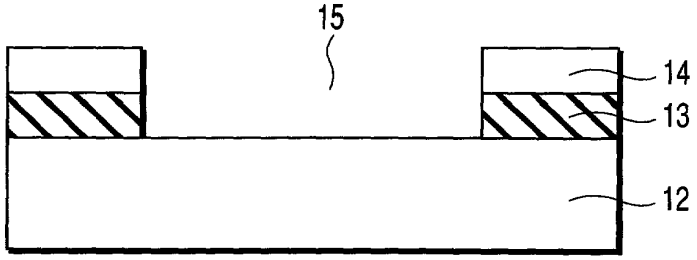


FIG. 1D
PRIOR ART

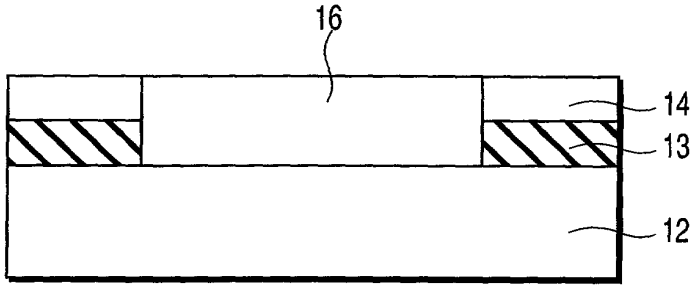
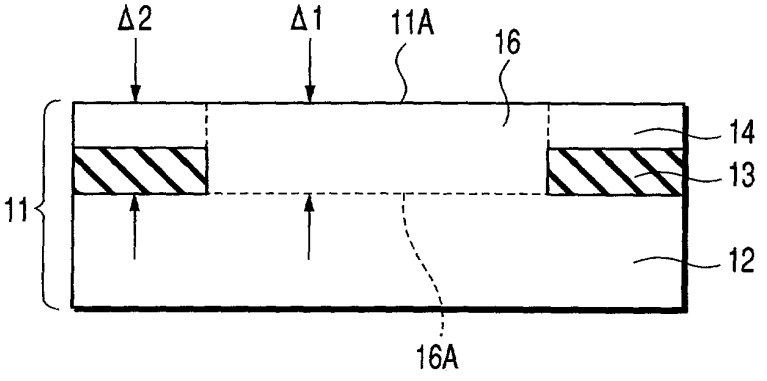


FIG. 2
PRIOR ART



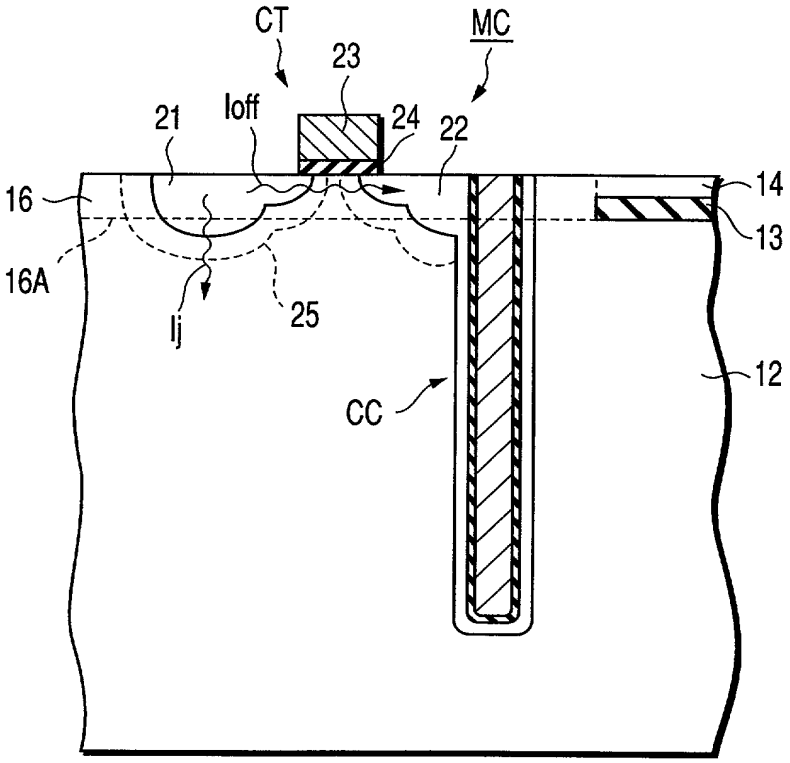


FIG. 3
PRIOR ART

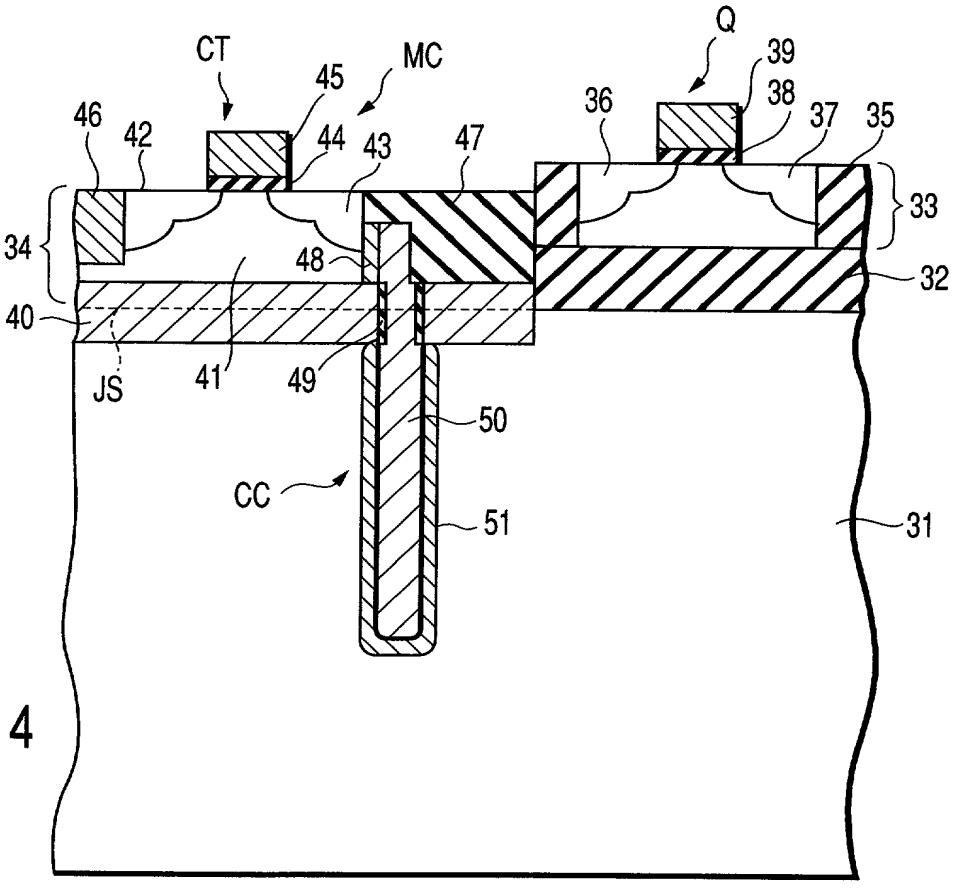
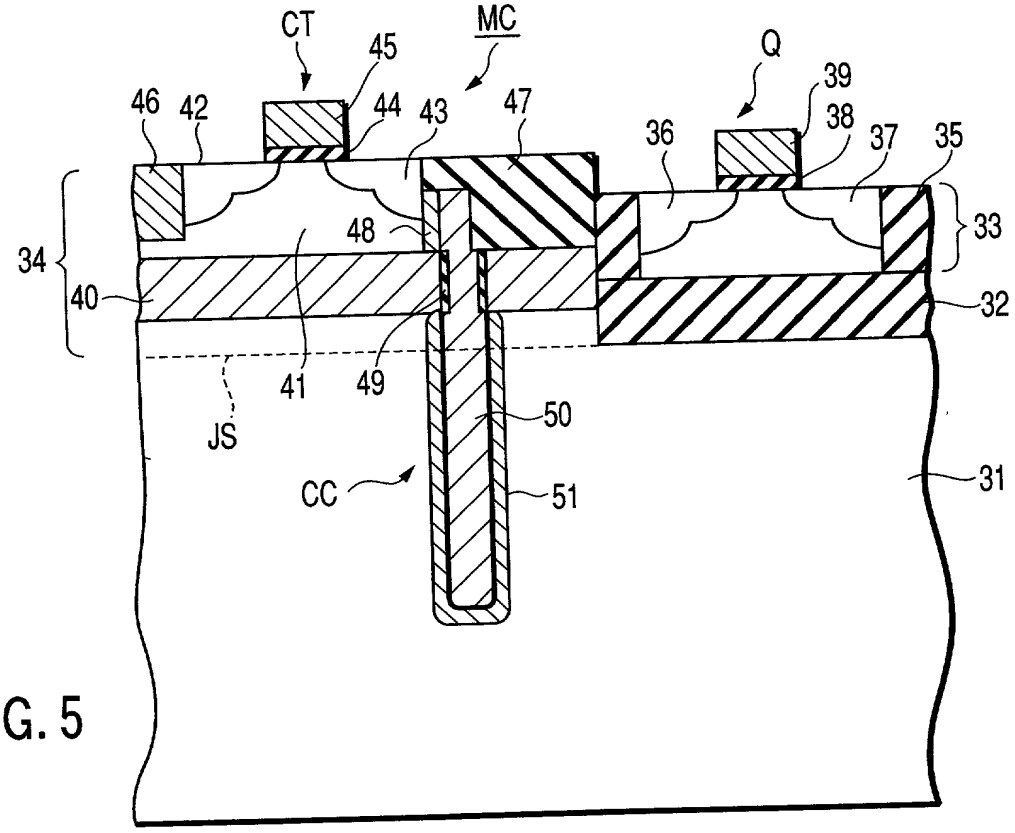


FIG. 4


CT
MC
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Q
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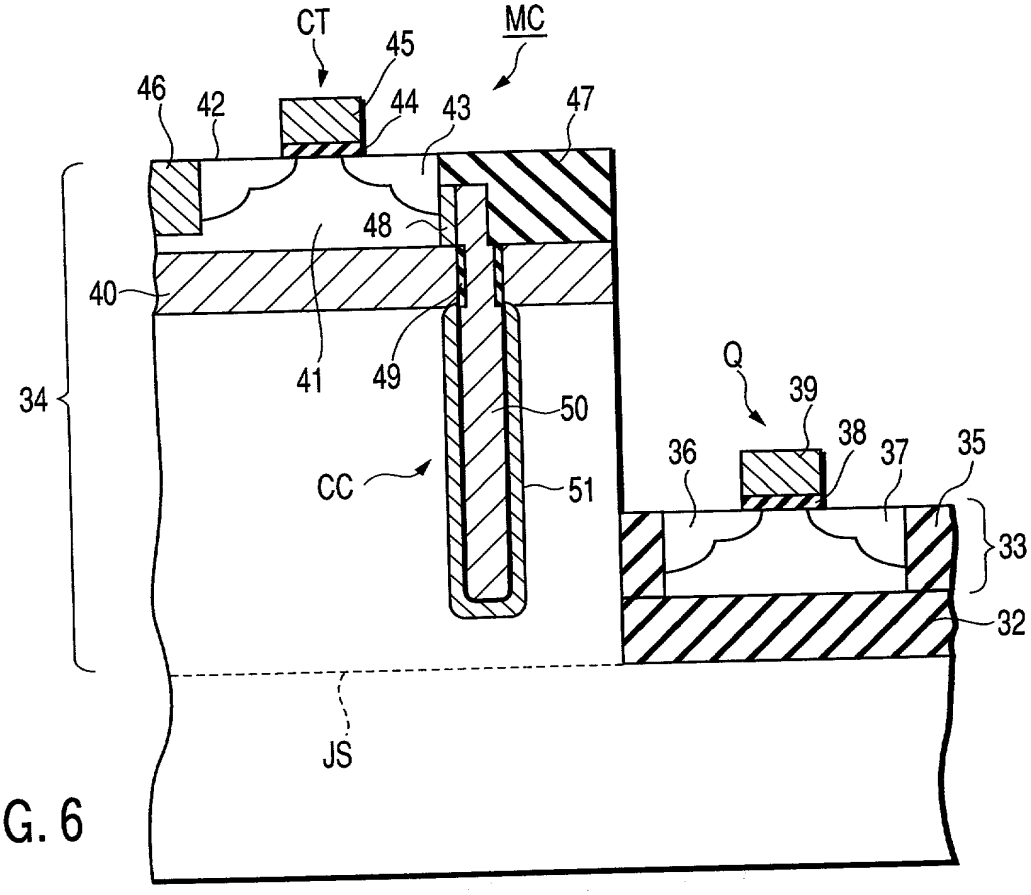
FIG. 5


CT
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32
JS

FIG. 6

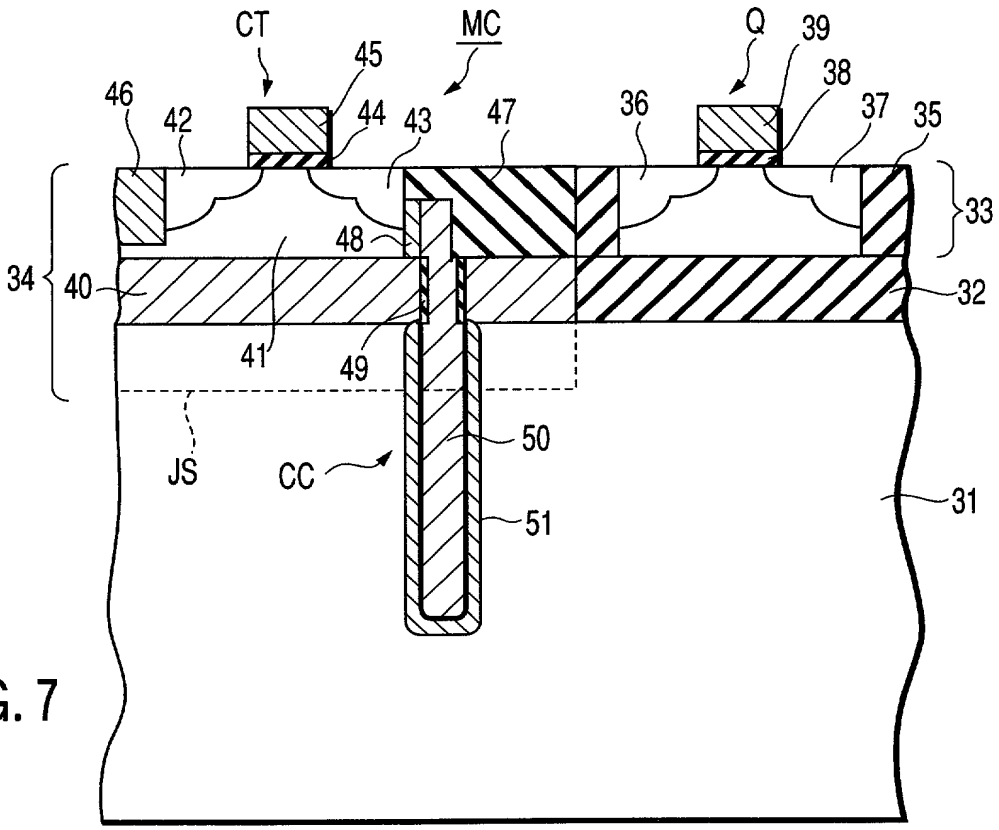
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FIG. 7

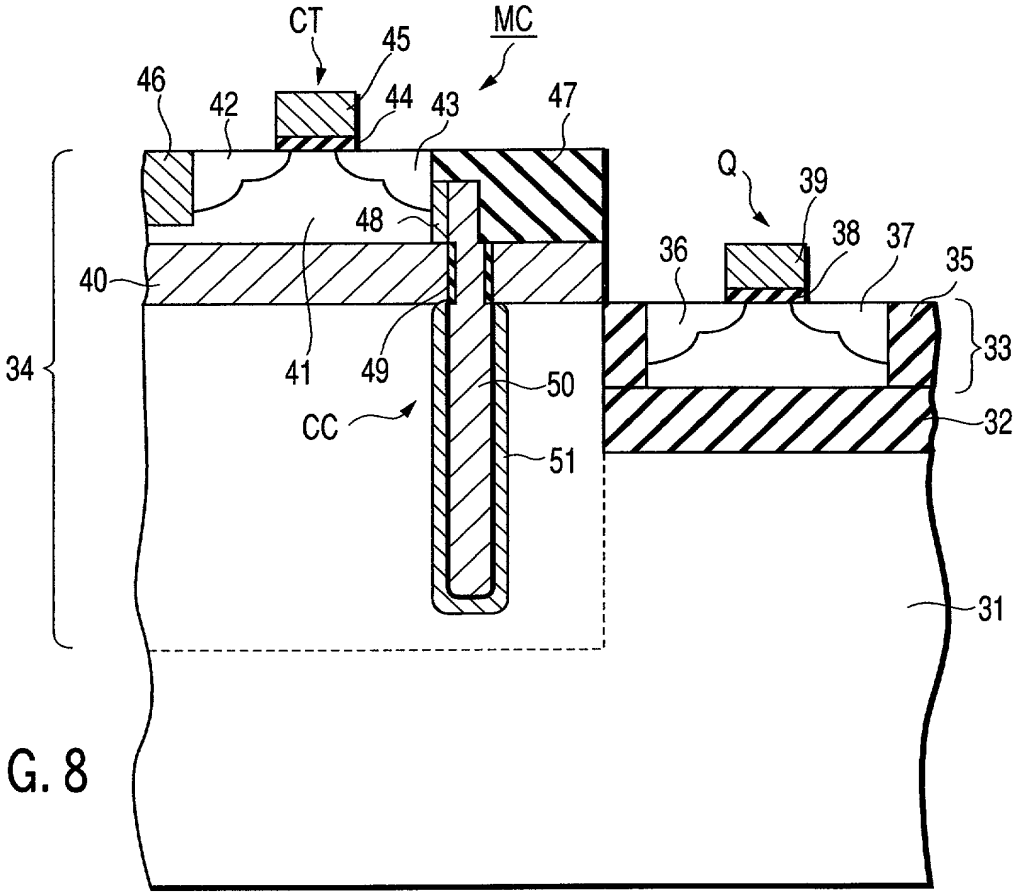
CT
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FIG. 8

FIG. 9A

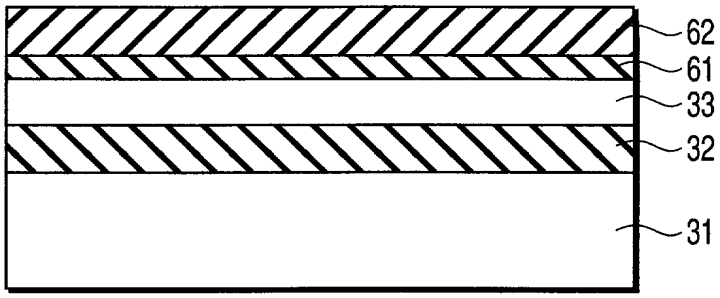


FIG. 9B

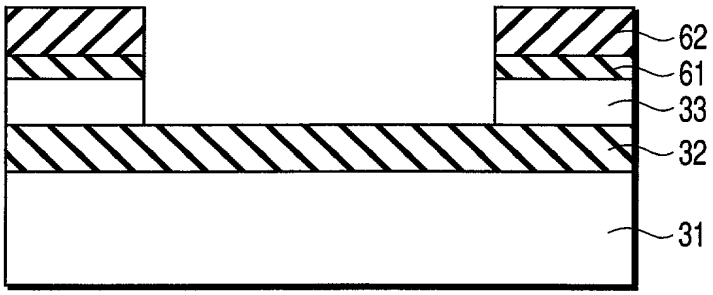


FIG. 9C

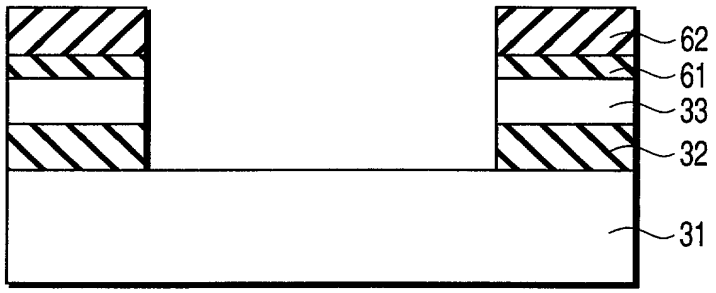
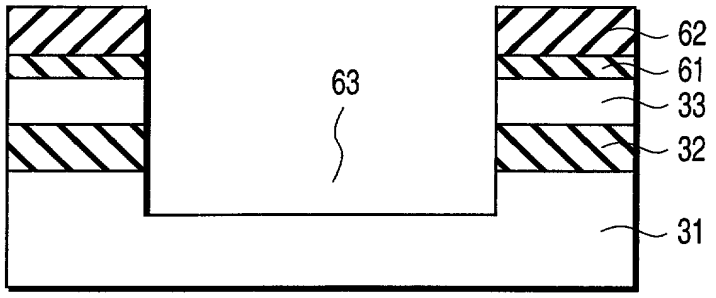


FIG. 9D



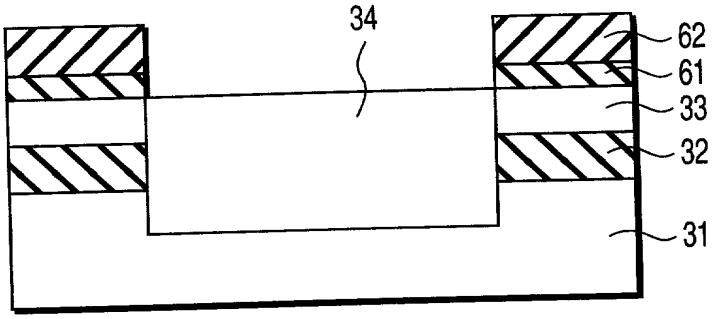


FIG. 9E

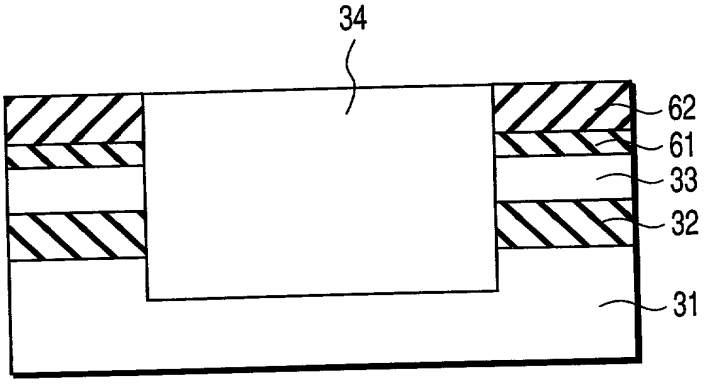


FIG. 10

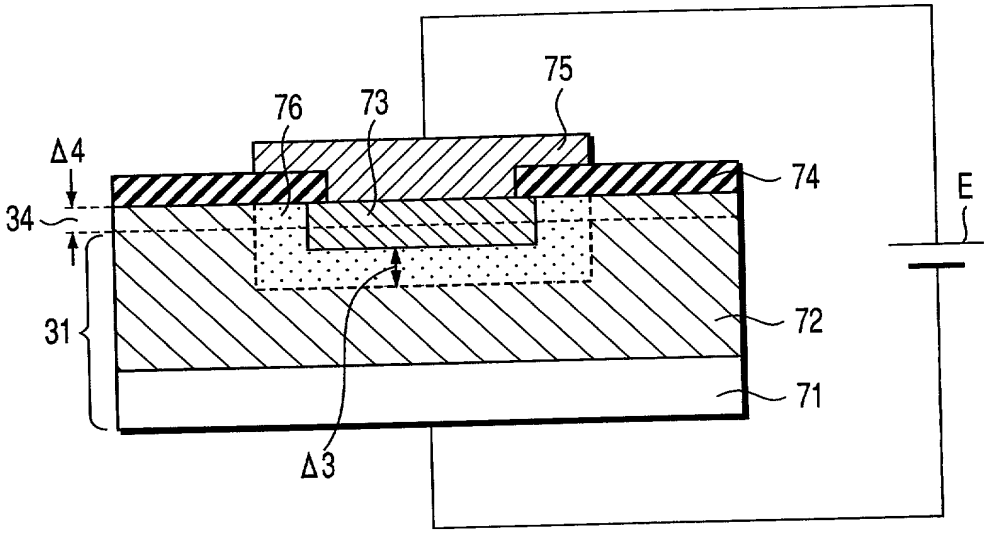


FIG. 11

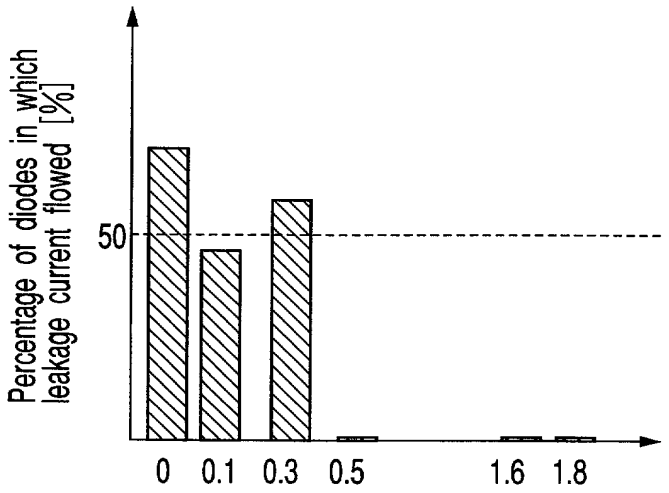

Percentage of diodes in which leakage current flowed [%]
50
0
0.1
0.3
0.5
1.6
1.8
Thickness of silicon layer Δ4 [μm]
Reverse bias: 2V (Width of depletion layer Δ3: 0.25μm)

FIG. 12

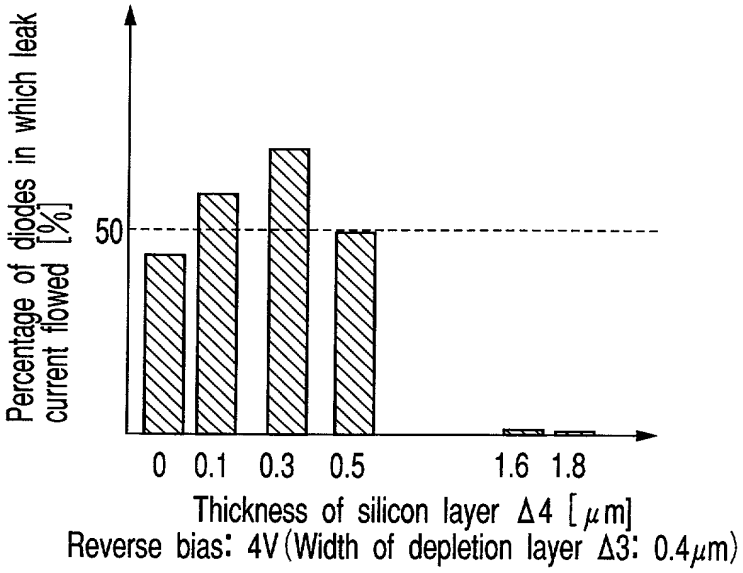

Percentage of diodes in which leak current flowed [%]
50
0
0.1
0.3
0.5
1.6
1.8
Thickness of silicon layer Δ4 [μm]
Reverse bias: 4V (Width of depletion layer Δ3: 0.4μm)

FIG. 13

RE1: Leakage current when thickness of silicon layer is set at 0, 0.1, 0.3 μm
RE2: Leakage current when thickness of silicon layer is set at 0.5 μm
RE3: Leakage current in this embodiment (when thickness of silicon layer is set at 1.6, 1.8 μm)

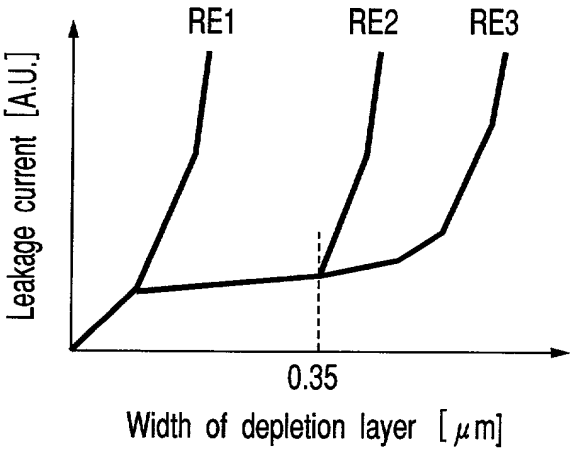


FIG. 14

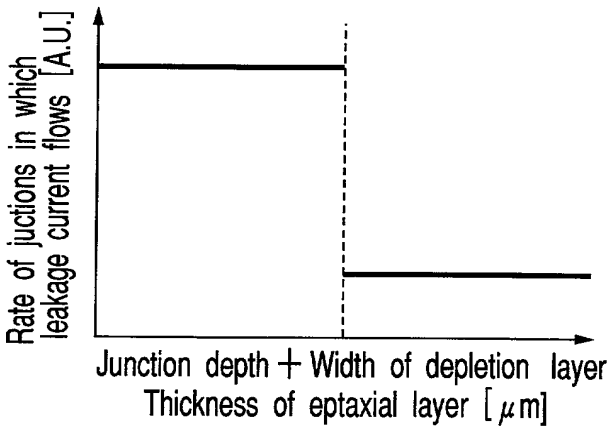


FIG. 15

FIG. 16A

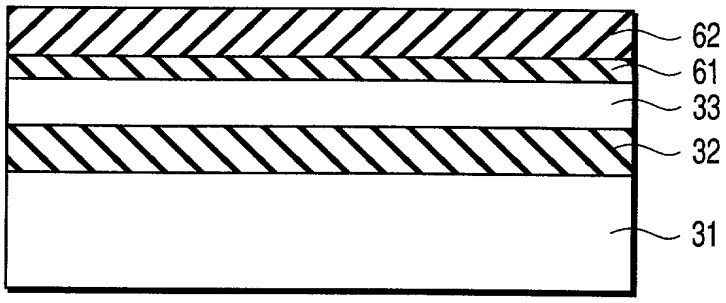


FIG. 16B

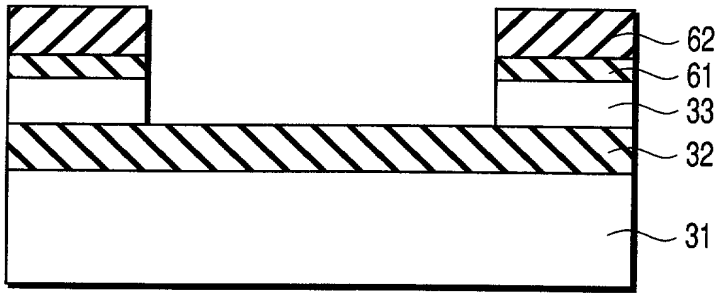


FIG. 16C

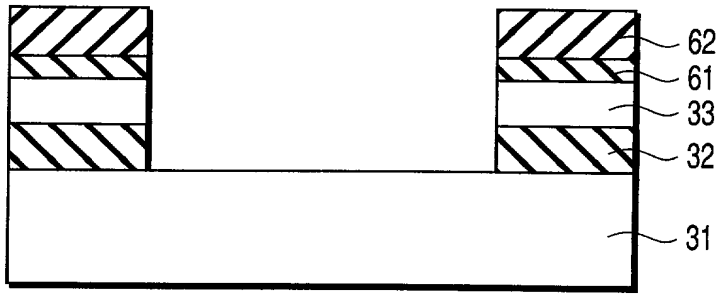


FIG. 16D

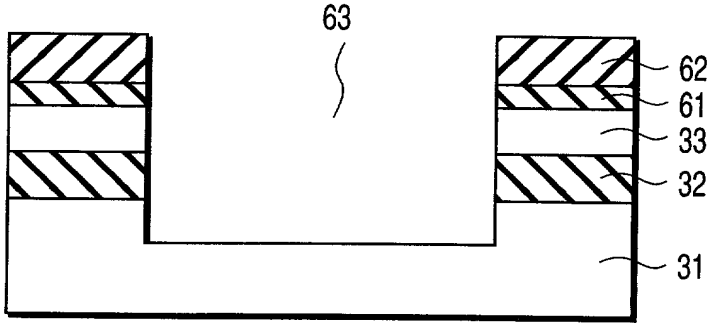


FIG. 16E

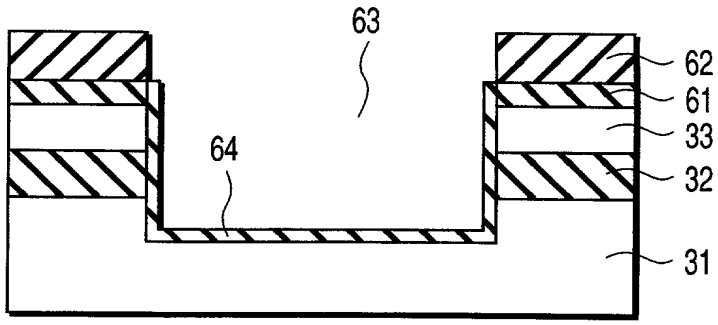


FIG. 16F

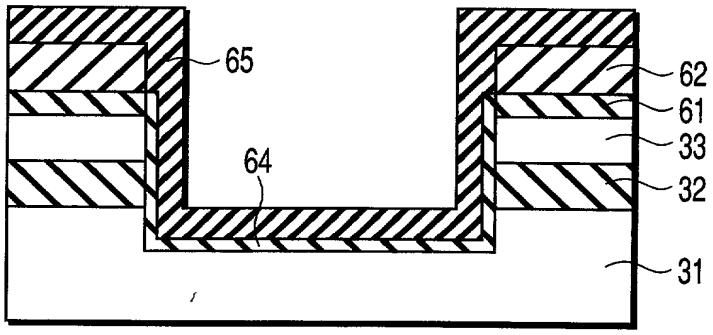


FIG. 16G

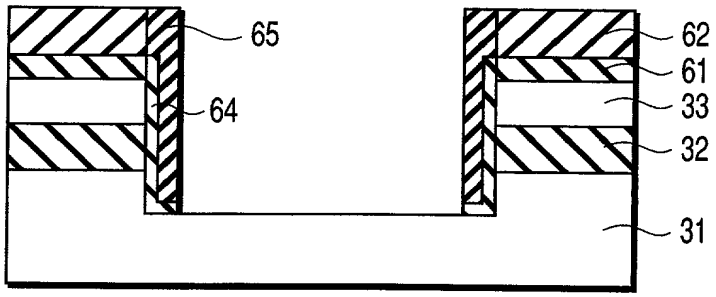


FIG. 16H

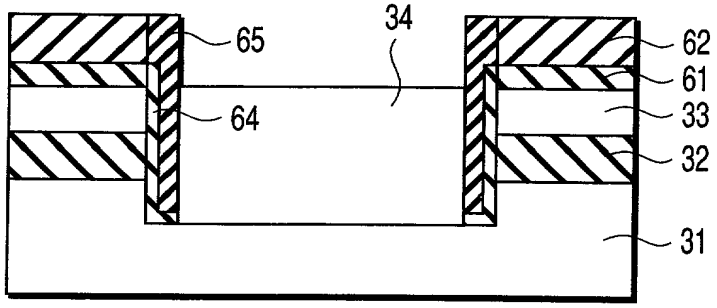


FIG. 17

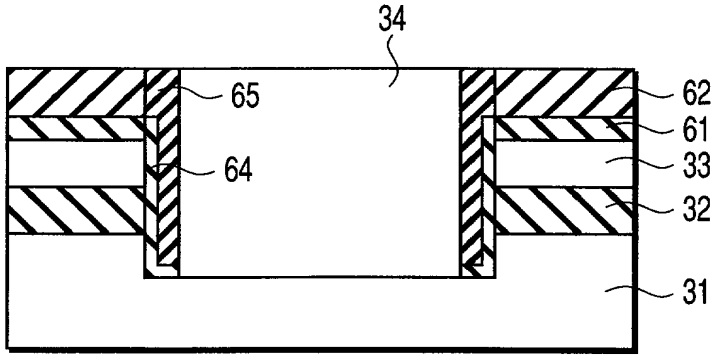


FIG. 18A

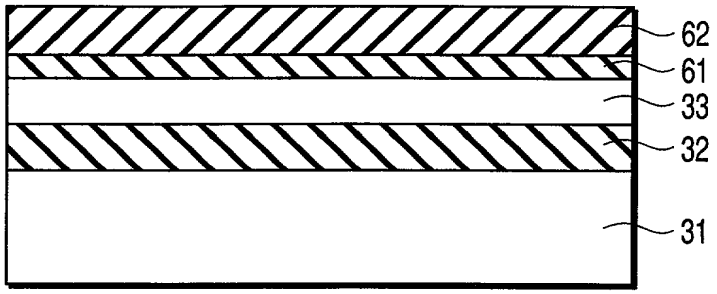


FIG. 18B

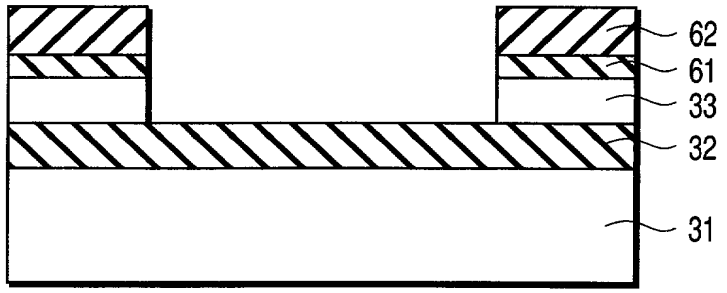


FIG. 18C

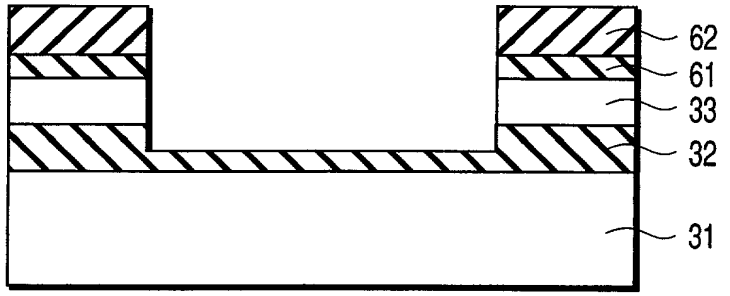


FIG. 18D

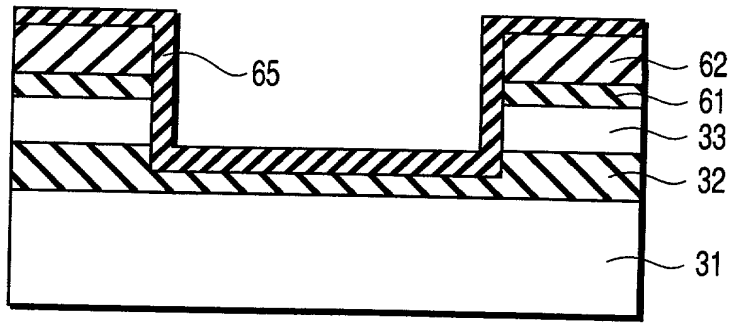


FIG. 18E

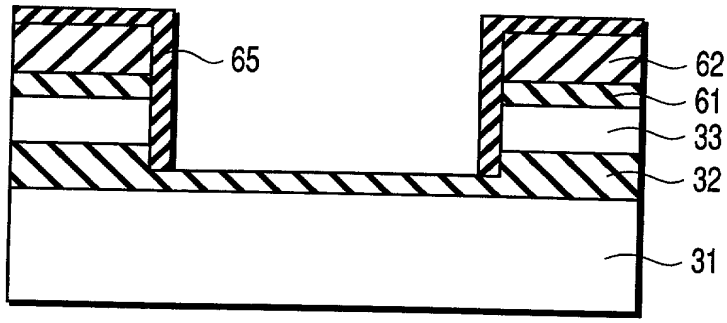


FIG. 18F

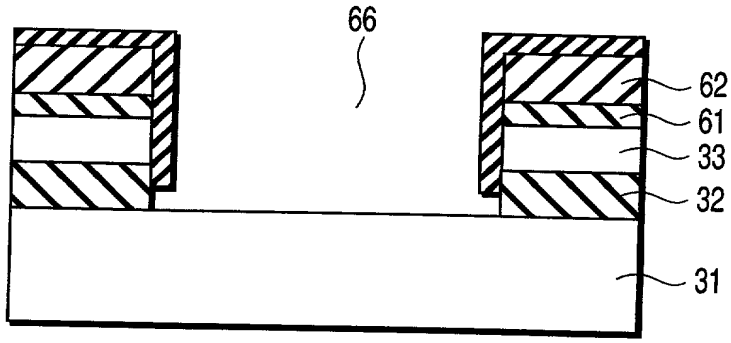


FIG. 18G